Analysis and Evaluation of Adiabatic PFAL Inverter

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Abstract: In this paper authors have investigated thoroughly the semi adiabatic PFAL based basic inverter implementation for its working. The said circuit is analyzed for different transistor size, frequency, charge transfer time-rate, load capacitance, for different parameters related to delay, power, power delay product, rise time, fall time, etc. The PFAL based inverter circuit is analyzed for said parameters taking 20 different transistor sizes namely 1.8µm, 3.6µm, 5.4µm, 7.2µm, 9.0µm, 10.8µm, 12.6µm, 14.4µm, 16.2µm, 18.0µm, 19.8µm, 21.6µm, 23.4µm, 25.2µm, 27.0µm, 28.8µm, 30.6µm, 32.4µm, 34.2µm, and 36.0µm and 11 different loads namely 0.1pF, 10.1pF, 20.1pF, 30.1pF, 40.1pF, 50.1pF, 60.1pF, 70.1pF, 80.1pF, 90.1pF; for ‘out’ and ‘outbar’ terminals. The capacitance distribution and its effects are investigated in the circuit nodes are analyzed along with their effects on rise time, fall time of the output signals. The current drawn from the supply for different permutations of Cload and transistor size are analyzed along with the current feedback to the power supply. The average power distribution and maximum power distribution for the power source is also evaluated. The power delay product is also analyzed for different Cloads and transistor size which is further appreciated with input signal requirement analysis for effect of the circuit in the form of PDP calculation for V_in and V_inh signals. Finally the normalized power drawn from the power source and normalized power feedback to the power source is analyzed and studied for power feedback capabilities dependencies on transistor size and Cloading for the said circuit. Authors have also tabulated the PDP variation for Cload and transistor size which can be used for selecting the nearest best suitable transistor size for given design parameters.

Keywords: Low power, VLSI circuit design, Adiabatic logic circuit, PFAL semi adiabatic logic, inverter logic, circuit investigation.

1. INTRODUCTION

Since last decade there is tremendous shift in the circuit design approach in which power equation is now one of the essential primary considerations, as compared to the era few times before where speed and features counts are the main considerations. This shift is obvious because of the numerous advancements in different related technologies and also changes in the customer’s needs and demands which govern the IC market. Wishlist of the customer is growing in different dimensions challenging the technology in every sphere. The simple speed, power and area trade-off theories based concepts are hard to find acceptance in market. The desire of having best optimized solution to their requirements over-suits the prior theories and predictions. The growth and requirement of functionality needs in the electronic products are exponential which in turn increases the complexity level of the IC design tremendously. Hence the transistor count is beyond predictions and now products are approaching and passing the day-old boundaries/rule proposed by “G Moore” [3-6] in his famous “Moore’s Law” which find its
existence and acceptance in last 50-60 years unchallenged. Scaling technologies are also approaching to their limits in current physical, structural domains. Transistor sizing and Voltage Scaling along with other power optimizing techniques proved to be a boon and has played a very critical role in producing very-very complex ICs fulfilling the market needs and in many applications over passing the expectations of the users by higher degree of margin in positive levels [7-10]. The chip cooling technology depending upon the laws of physics and thermodynamics faces volcanic challenges in cooling the system involved when the per unit area heat dissipation is reaching to the levels that of nuclear reactor and sun planet. These challenges have made advancements in this sphere; in-sufficient while dealing with said boundaries [10-13]. Seeing the positive aspect of the new advanced Battery Related Technologies which assisted this growth path, showcase a very lucrative and acceptable picture but on the other hand, rate of their advancements and their limitations in terms of chemical, physical science have also paralyzed the product development process and many a times become major hindrance in the realization of an ambitious concept. Enormous amount of computations in the complex products have affected the environmental temperature directly and indirectly. Not only a substantial amount of heat is dissipated due to these but also due to different cooling mechanisms adopted to eradicate the heat from immediate vicinity in turn further complicates gigantic problem involved. In view of the shrinking capabilities of various technologies involved IC designers, scientist, researchers are compelled to bring innovative solutions capable of addressing the complex issues of multifunctional high performance power aware IC development process. In pursuit of the same the adiabatic logic based circuit design tries to address the issue to a substantial extent for different application-al approaches with power aware designs trading the other parameters [14]. In the presented work authors have regously investigated the basic inverter circuit of semi adiabatic PFAL family for suitability and applicability of the design with different parameters. The different boundaries of operations for the circuit are tried to be drawn via the analysis process of the results obtained.

Chapter 2 provides the basics of the adiabatic logic transfer process. The PFAL semi adiabatic is also explained here. Chapter 3 discusses the implementation and different analysis made. Results from the analysis are drawn in chapter 4. Finally the presented work is concluded.

2. ADIABATIC LOGIC TRANSFER

2.1. Adiabatic process and adoption in VLSI

The term adiabatic came from ‘adiabatos’ a greek word which means zero energy exchange with the environment leading to no energy loss as heat dissipation. This principal is inherently used in thermodynamics for efficient design problems. In modern day when design industry is approaching limits of the traditional low power techniques, scientist and researchers in the area have borrowed the adiabatic concepts for lower down the power equations involved in chip design. The adoption of adiabatic process for VLSI is way back 10-15 years before but due to speed requirements it could not attract the community then. Now lot of work is being done on this, designers find it quite useful technique for power aware design process. The adiabatic logic family circuits are also many times named as ‘energy recovery’ or ‘charge recovery’ circuit. They make use of the charge stored on the nodes in circuit for later use instead of dissipating them to ground nodes. Adiabatic logic family circuits are broadly classified as ‘quasi-adiabatic logic circuits’ and ‘fully adiabatic circuits’, depending upon the capability of the family to take care of adiabatic energy loss. Quasi adiabatic logic circuits dissipate non-adiabatic energy during the operations mainly because of capacitance involved and voltages levels.

2.2. Logic Transfer Process

As a revisit to the conventional logic transfer mechanism in static CMOS family circuits consider the following examination for charging and discharging of the output capacitor and power drawn from the power source which is dissipated to the ground path. The conventional static CMOS circuit contains a ‘P network’ and a ‘N network’. ‘P network’ is responsible transferring logic 1 at the output node connecting the output node with the power supply depending upon the input vectors permutations as depicted in figure 1. The ‘N network’ is responsible for logic ‘0’ at the output node connecting the output node with the ‘gnd’ terminal and hence discharging the charge stored at load capacitance. Switching Power Dissipation (SPD) for Static CMOS (SCMOS) family is given by equation 1.
\[ P_{\text{DISSIPATED}} = \frac{1}{2} (C_{\text{LOAD}} V_{\text{SUPPLY}}^2 F \alpha_{\text{ACTIVITY}}) \]  

\[ \therefore P_{\text{DISSIPATED}} \propto \frac{1}{2} (C_{\text{LOAD}} V_{\text{SUPPLY}}^2) \]  

For unity product factor of frequency and activity equation 2 shows the direct proportionality of the SPD on the load capacitance and square of power supply voltage level. This proves to be limiting factor or minimum limit for the SPD in case of SCMOS family based circuits. Adiabatic logic transfer tries to lower this limiting lower boundary for the logic implementation utilizing the adiabatic approach while transferring the logic levels in-between the circuit nodes. Also the power dissipated due to current flow through a resistance as in figure 2a is depicted in equations 3 to 5. Total power dissipated during infinite time duration is zero as shown in equation 6 and equation 7.

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\[ P_{\text{RESISTANCE}} = V_{\text{DIFFERENCE}} I_{\text{FLOWING}} \]  

\[ V_{\text{DIFFERENCE}} = I_{\text{FLOWING}} R \]  

\[ P_{\text{RESISTANCE}} = I_{\text{FLOWING}}^2 R = V_{\text{DIFFERENCE}} I_{\text{FLOWING}} \]  

\[ P_{\text{TOTAL (t1 TO t2)}} = \frac{1}{(t2 - t1)} \int_{t1}^{t2} v(t)i(t)dt \]  

\[ \lim_{t2 \to \infty} (P_{\text{TOTAL (t1 TO t2)}})^n = 0 \]  

Therefore it can be inferred that power boundaries can be reduced by decreasing the logic transfer rate as illustrated in figure 2b, with time-variant source for R and C network. The time variant source \( v(t) \) used for charge transfer with quite low value for \( dv(t)/dt \), equation 8 to equation 10 shows the time dependency of the current passing through. Pursuing the process further through equation 11 to equation 13, the power controlling parameter associated are: capacitance, supply voltage, time, and resistance. For \( T > 2RC \) energy associated would be less than conventional charge flow process along with other concerned parameters.

\[ v(t) : V_{\text{DD}} \]  

\[ T \]  

\[ v(t) \]  

\[ i(t) \]  

\[ v(t) \]  

\[ v_{\text{C(t)}} \]  

\[ v_{\text{C(t)}} \]
\[ v_C(t) = v(t) = \frac{1}{2} i(t) \]  
\[ i(t) = \frac{C_v(t)}{t} \]  
\[ i(t) = C \frac{dv(t)}{dt} = \frac{CV}{T} \]  
\[ E = \int_0^T v(t) \times i(t) \, dt = \int_0^T \left[ \{V_R(t) + V_C(t) \} \times i(t) \right] \, dt \]  
\[ VR(t) = i(t)R \]  
\[ E = \int_0^T R \frac{C^2V^2}{T^2} \, dt = \frac{RC}{T^{CV^2}} \]

2.3. PFAL Semi Adiabatic family

The block level depiction for the PFAL based circuit implementation is shown in figure 3. It contains cross coupled invertors. The logic is implemented using N transistors both for primed and unprimed functionalities which are connected between power clock and output nodes as shown. As the Nmos transistors are used for mapping the logic data ‘1’ at the output, full swing cannot be achieved through the network but mapped because of cross coupled inverter stages. Also the transistor count is high as compared to the conventional CMOS based implementation for the same functionality. PFAL family is similar to ECRL family where the latch structure is made up of two P transistors only [14-16].

3. IMPLEMENTATION AND ANALYSIS

A four phase power clock as shown in figure 4 is used to drive the circuit. In the first ‘Evaluate phase’ the logic of the circuit is evaluated based upon the input values. Second ‘Hold phase’ hold the evaluated value in the circuit processing. In third ‘Recovery phase’ the charge from the circuit is recovered back to the reservoir for further utilization in subsequent stages. In fourth ‘Ideal phase’ the transistor terminals are at same levels leading to no current; and next input levels may be provided in the ideal phase. The implementation parameters are listed into Table 1. The circuit simulation waveforms are shown in figure 5.

Fig. 4. Four phase power clock PCLK.
Table 1. Simulation parameters.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Value</th>
<th>Simulation</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Length</td>
<td>.180 microns</td>
<td>Power clock</td>
<td>pulse type with Trise and Tfall</td>
</tr>
<tr>
<td>Min. width</td>
<td>.180 microns</td>
<td>Input Signal</td>
<td>Bit type</td>
</tr>
<tr>
<td>Max. width</td>
<td>36 microns</td>
<td>Delay calculation</td>
<td>50% points</td>
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<tr>
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<td>V_{ton}</td>
<td>$</td>
<td>0.3932664</td>
</tr>
<tr>
<td>TOX</td>
<td>4.10E-09</td>
<td>Power clock Time period</td>
<td>40 micro sec</td>
</tr>
</tbody>
</table>

MOS Gate Capacitance Model: capmod = 0; Conditions: Voltage – Upto 5 V max; Temperature – 25 degree C

4. RESULTS

The capacitance distribution in the circuit topology is shown in figure 6 and 7. It can be inferred that when Cload is high the contribution of the parasitic at nodes ‘IN’, ‘INB’ and ‘PWR’ are nullified. 50% of the contribution is at the discharging path of the circuit. Remaining 50% is contributed by the Cload at the ‘out’ and ‘outb’ nodes. On the other hand for lower Cloads the node capacitance at ‘PWR’, ‘IN’ and ‘INB’ are quite countable. It is also evident from the circuit topology analysis that with increase in load the effect of the width on the ‘GND’ capacitance becomes negligible. Circuit has two ‘GND’ paths with two NMOS transistors of the two cross coupled inverter. The capacitance involved in the path would be from one path at a time as only one NMOS transistor would be on discharging the charge to ‘GND’. The ground capacitance can be depicted as illustrated in equations 14. Where ‘p’ and ‘q’ are contributory factors for cross coupling of the inverter to the respective gate and drain terminals of the transistors.

\[
C_{g_{nd}} = C_{gs1} + C_{bs1} + C_{ds1} + C_{ds2} + pC_{ds2} + qC_{ds2} + C_{int} \tag{14}
\]

Now as C_load is connected to the ‘out’ and ‘outb’ terminals, hence \(C_{outb}\) and \(C_{out}\) are equivalent to \(C_{load}\).

\[
\therefore C_{g_{nd}} = C_{gs1} + C_{bs1} + C_{gs2} + C_{int} + (1 + p)C_{load} \tag{15}
\]

\[
\therefore C_{g_{nd}} \Delta zC_{load} \tag{16}
\]

\[\because\] as the \(C_{load}\) increase the parasitic of the transistor looses their impact on the ‘GND’ path.
For the complete cycle flow the \( C_{\text{gnd}} = 2C_{\text{gnd}} \) and \( C_{\text{gnd}} \) is responsible for non adiabatic loses in the circuit. Also it is evaluated from the circuit topology that the ‘PWR’ node has around 4 times the capacitance at the input nodes.

Figure 8 shows the variation of rise time (\( T_{\text{rise}} \)) and fall time (\( T_{\text{fall}} \)) for the ‘Out’ and ‘Outb’ terminals of the circuit with different \( C_{\text{loads}} \) and transistor size. As the transistor size increases the variation in the \( T_{\text{rise}} \) and \( T_{\text{fall}} \) reduces which is maximum for lower size transistors and higher \( C_{\text{load}} \) values. It is evident from the chart that \( T_{\text{fall}} \) gets reduced exponential and \( T_{\text{rise}} \) increases exponential after certain points for lower transistor size. On the other hand the \( T_{\text{rise}} \) and \( T_{\text{fall}} \) are equal for higher transistor size for a given \( C_{\text{load}} \) value. For lower transistor size and higher \( C_{\text{load}} \) the variation of \( T_{\text{rise}} \) and \( T_{\text{fall}} \) is quite large as compared to larger transistor operating in circuit. It can be concluded that for higher \( C_{\text{load}} \) value larger transistors should be used to minimize the variation of \( T_{\text{rise}} \) and \( T_{\text{fall}} \).

The current drawn from the ‘PWR’ power clock source and current feedback to the supply ‘PWR’ have small deviation as shown in figure 9. This current value is responsible for the non adiabatic loss through the \( C_{\text{gnd}} \) ground node capacitance. As evident from the graph with increase in size of the transistor the current drawn from the source increases and hence power drawn. Also the current feedback to the source also increases with transistor size. As evident a linear approximation may be considered for analyzing the relationship of supply current and transistor size.

Also the window of the variation of current with \( C_{\text{load}} \) increases with the transistor size. So wider is the transistor size more is the variation of the current supplied by the source with \( C_{\text{load}} \) values. Also the amount of deviation of the two set of curves for current supplied and current feedback the deviation amount is less for current feedback as compared to current supplied. This means the dependencies of the current feedback to supply on the transistor size is less variant with \( C_{\text{load}} \) and certain amount of current out of total current supplied contributes to the non adiabatic losses in the circuit.

The average power distribution with transistor size and \( C_{\text{load}} \) is shown in figure 10. With increasing transistor width after size 7 units the \( P_{\text{avg}} \) can be approximated to be linear and more or less constant. So with the increase in size of the transistor the \( P_{\text{avg}} \) decreases to a limiting value forming a curved L shaped behavior. The exponential rise in \( P_{\text{avg}} \) with transistor size is more for higher \( C_{\text{load}} \) values as compared to lower \( C_{\text{load}} \) values. Also with increase in \( C_{\text{load}} \) the curve offset showing direct relationship of \( P_{\text{avg}} \) and \( C_{\text{load}} \) upto loading of 20pF, the \( P_{\text{avg}} \) distribution is more or less linear with transistor size and one can approximate \( P_{\text{avg}} \) as constant for this \( C_{\text{load}} \) with variation in transistor size. It can be inferred that there is direct relationship between \( C_{\text{load}} \) and \( P_{\text{avg}} \) (lesser the \( C_{\text{load}} \) lesser the \( P_{\text{avg}} \)). The window for variation in \( P_{\text{avg}} \) for different transistor width is less for higher transistor width and more for less transistor width. It can be inferred as known earlier if the \( C_{\text{load}} \) is higher the one should use wider transistor to dissipate less power which can be reduce at wider transistor by a factor of 6-8 % percent at less wider transistor.

Also as input signal has to drive circuit input capacitance. Hence the power dissipation wrt \( V_{\text{in}} \) is also analyzed for the circuit topology. It is seen that \( P_{\text{avg}} \) wrt \( V_{\text{in}} \) is depending upon the transistor width. The variation in \( P_{\text{avg}} \) wrt \( V_{\text{in}} \) with \( C_{\text{load}} \) is negligible i.e. making the contribution of the input sources for load driving negligible. The input source are used inherently to drive the transistors and hence higher the width more the power drawn from input source. It can be inferred higher the transistor width more the power drawn from the source to drive them i.e. stronger input signal is required for larger transistor in the circuit. The divergence of the \( P_{\text{avg}} \) from \( V_{\text{in}} \) source is very less which is negligible contribution.

The max power drawn from \( V_{\text{puls}} \) is more or less constant with some deviation when seen for certain \( C_{\text{load}} \) as evident in figure 11. Hence the max power taken can be considered independent of transistor width. Also we have direct relationship for \( P_{\text{max}} \) with \( C_{\text{load}} \) i.e. higher the \( C_{\text{load}} \) higher the \( P_{\text{max}} \). As shown in figure 12 the \( P_{\text{DP}} \) increases with increase in transistor width and the rate of increase is more or less same for different \( C_{\text{load}} \) values. But the offset value by which the \( P_{\text{DP}} \) shift in accordance with the \( C_{\text{load}} \) change increases with the increasing \( C_{\text{load}} \) value.

So less the transistor size for a given Cload lesser would be the PDP. As it should be and shown in figure 13 the PDP value wrt to \( V_{\text{in}} \) are more or less independent of \( C_{\text{load}} \) values and are parabolic in nature for transistor width variation. For higher transistor size beyond 12.6¼ the PDP variation curve offers some offset with lower transistor.
size. The PDP distribution is also tabulated in table 2. For $V_{\text{puls}}$, $V_{\text{in}}$ and $V_{\text{inb}}$ considering the $V_{\text{in}}$ to ‘outb’ and $V_{\text{inb}}$ to ‘out’ delays. Through this depending upon the input strength availability and desired power supply dependent PDP and output loading required the transistor size can be considered for the circuit implementation.

Figure 14 shows the variation of power drawn from the $V_{\text{puls}}$ source and the power feedback to the $V_{\text{puls}}$ source for 1V trapezoidal supply. ‘Pd’ depicts the power drawn and ‘Pf’ depicts the power feedback. Numeric values appended after ‘Pd’ and ‘Pf’ depicts the value of the $C_{\text{load}}$ to the circuit output out and ‘outbar’ terminal. The variations are drawn for different transistor size at the x-axes. From the graph it can be inferred straightforward that as the size of the transistor increases the power dissipation increase as expected. The difference in the ‘Pd’ and ‘Pf’ values which is most evident for $C_{\text{load}}$ 0.1pF, shows the power lost in the system which could not be recovered adiabatically. In some cases due to past charge storage at the intermediate nodes the power feedback to the supply approaches equivalent values to that of power drawn from the supply because of the residual storage of charge in the intermediate nodes of the past charge flow cycles according to the input values there as is evident for $C_{\text{load}}$ 10pF. The access feedback power is more for transistor size 10pF and as the size increases the difference increases perhaps due to more storage capacity with the transistor size. Also the variation of the power dissipation with $C_{\text{load}}$ is less as the load value increases after 10pF. The average power consumption wrt $V_{\text{puls}}$, $V_{\text{in}}$ and $V_{\text{inb}}$ are 0.65nW, 0.045nW, 0.23nW respectively. Also the Small Signal Transfer Function parameters for the circuit are summarized before:

$$v(\text{OUT}) / V_{\text{IN}} = -2.0405e-051$$
$$v(\text{OUTB}) / V_{\text{IN}} = 8.3013e-023$$
$$v(\text{OUT}) / V_{\text{INB}} = -5.8005e-017$$
$$v(\text{OUTB}) / V_{\text{INB}} = 4.8152e-039$$

Output resistance at $v(\text{OUT}) = 6.3584e+002$
Output resistance at $v(\text{OUTB}) = 2.1473e+009$

5. CONCLUSION

In the presented work authors have analyzed the circuit performance parameters for semi adiabatic PFAL inverter proposed by Vetuli, Pascoli and Reyneri evaluating the positivities of feasibility for implementing the circuit on 180nm technology. The said circuit is analyzed for 20 transistor sizes namely 1.8µm, 3.6µm, 5.4µm, 7.2µm, 9.0µm, 10.8µm, 12.6µm, 14.4µm, 16.2µm, 18.0µm, 19.8µm, 21.6µm, 23.4µm, 25.2µm, 27.0µm, 28.8µm, 30.6µm, 32.4µm, 34.2µm, and 36.0µm. 11 loads namely 0.1pF, 10.1pF, 20.1pF, 30.1pF, 30.1pF, 40.1pF, 50.1pF, 60.1pF, 70.1pF, 80.1pF; for ‘out’ and ‘outbar’ terminals. The capacitance distribution in the circuit nodes is analyzed along with their effects on rise time, fall time of the output signals. The current drawn from the supply for different permutations of $C_{\text{load}}$ and transistor size are analyzed along with the current feedback to the power supply. The average power distribution and maximum power distribution for the power source is also evaluated. The power delay product is also analyzed for different $C_{\text{loads}}$ and transistor size which is further appreciated with input signal requirement analysis for effect of the circuit in the form of PDP calculation for $V_{\text{in}}$ and $V_{\text{inb}}$ signals. Finally the normalized power drawn from the power source and normalized power feedback to it is analyzed and studies for power feedback capabilities dependencies on transistor size and Cloading for the said circuit. From the analysis it can be concluded that for loads the power supply and input needs a countable share of total capacitance distribution as compared to for higher loads where their contribution can be neglected. Also while ground path capacitance acts as output for non-adiabatic power dissipation by the circuit. It can be further concluded that for lower transistor size and higher $C_{\text{load}}$ the variation in rise time and fall time are quite large hence this combination should not be used while implementing the circuit for keeping the rise time fall time variance at minimum, which can be achieved using larger size transistor with wise range of $C_{\text{load}}$ capabilities.

The conclusion can be extended for current drawn from the power source and feedback to it. For larger size transistor the current variation supplied is more which can be analyzed on a linear scale. The capabilities of the circuit to feedback to the power source depend greatly on transistor size as compared to applied. Also it can be
concluded that average power reduces a limiting valued following a ‘L’ shaped curve behavior. The direct relationship of average power for $C_{\text{load}}$ transistor size is evident for higher loading the contribution of power dissipation by the transistor parasitic reduces as compared to the contribution of load capacitance. Also for higher $C_{\text{load}}$ less power dissipation can be achieved using wider transistor width factor of 6-8% reduction in power equations. Subsequently stronger input signals have to be used for driving the larger transistors in efficient operation as analyzed using power calculations for input source. The maximum limiting power drawn from the source can be considered independent of transistor size and wholly dependent on $C_{\text{load}}$. The PDP calculations for the input signal are approximately independent of $C_{\text{load}}$ and depend on transistor size. For higher transistor size beyond 12 micron PDP shows offset for lower transistor size. Authors have also tabulated the PDP distribution for two $C_{\text{load}}$ at two transistor size which can be used for approximating the size of the transistor for the given design parameters constraints in terms of PDP. For some operations the power feedback to source approaches equivalent levels to that of power supplied making use of residual charge stored for $C_{\text{load}}$ 10pF. The variation in ‘$P_d$’ and ‘$P_f$’ becomes evident for $C_{\text{load}}$ beyond 0.1pF where non adiabatic loss is increased. The power feedback is more for transistor size upto 10micron and difference increase beyond 10micron size.

6. REFERENCES