Design of a 100MHz Highly Linear Source-Coupled CMOS Voltage Controlled Oscillator

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Abstract: Voltage controlled oscillators (VCO) are important building blocks in communication systems. In this paper design of a highly linear CMOS source coupled voltage controlled oscillator has been presented. The circuit has been simulated using BSIM4 model with 50nm CMOS process. Simulation results show that the centre frequency of the designed VCO is 100MHz at the input voltage of 0.45 volt. The maximum frequency is 112MHz and minimum frequency of 86 MHz has been reported. The gain of the VCO is $5.65 \times 10^9$ radians/Vs.

Keywords: CMOS; Voltage controlled oscillator; source-coupled.

1. INTRODUCTION

Oscillators are the important building blocks of the most of the electronic systems having a wide range of application in communication, control systems, signal processing, instrumentation and measurement systems [1]. In communication circuits' oscillators produce the continuous time periodic sinusoidal signals which are then modulated for the transmission over the channel. At the receiver end oscillators are required for the down conversion [2-5]. In instrumentation the oscillators are used in function generators to produce various waveforms used for testing. In signal processing they are used to produce signals for comparison and analysis of various signals under test [6-7].

In modern communication systems voltage controlled oscillators are used such as local oscillator in a communication transmitter, phase -locked loop (PLL) [8-10]. Many traditional oscillators are based on LC resonators. Due to the difficulties in the implementation of on-chip inductors and the limited frequency tuning range, resonator less VCOs have drawn significant attention for system-on-a-chip solutions [11-14]. The current trend of research is to design complementary metal-oxide-semiconductor (CMOS) VCOs for wireless applications [14-16].

In this paper design of a 100MHz source-coupled CMOS voltage controlled oscillator has been presented. The paper is organized in the following way. Section 2 contains the circuit of the designed CMOS voltage controlled oscillator. Finally section 3 shows the simulation results for the designed VCO circuit.

2. DESIGN OF CMOS VOLTAGE CONTROLLED OSCILLATOR

Figure 1 shows the schematic of the designed source coupled CMOS voltage controlled oscillator. MOSFETs named as $P_1$, $P_2$ and $N_1$, $N_2$ forms the current mirror circuit to mirror the desired current to the VCO. MOSFETs named as $N_3$ to $N_8$ forms the circuit of source coupled voltage controlled oscillator. In this circuit $N_3$ and $N_4$ behave as constant current sources which are sinking a current $I_D$. MOSFETs $N_5$ and $N_6$ operate as switches. If $N_5$ is on and $N_6$ is off, the drain of $N_6$ is pulled to $V_{DD}-V_{THN}$ by $N_7$. Since the gate of $N_5$ is at $V_{DD}-V_{THN}$, the source and drain of $N_5$ are $V_{DD}-2V_{THN}$. The output gate of $N_6$ is approximately $V_{DD}-2V_{THN}$ and is held at this voltage through $N_5$ until $N_6$ turns on and $N_5$ turns off. Initially when the MOSFET $N_6$ turns off and $N_5$ turns on, the node labeled $N_5$ is at $V_{DD}$. The current through capacitor causes node $N_5$ to discharge toward ground through MOSFET $N_3$. When the node $N_5$ gets down to $V_{DD}-V_{THN}$ the current through capacitor causes node $N_5$ to discharge toward ground through MOSFET $N_3$. The time taken by the node $N_5$ to change $2V_{THN}$ is given by:

$$\Delta t = C \cdot \frac{2V_{THN}}{I_D}$$  \hspace{1cm} (1)$$

Since the circuit is symmetrical, two discharge times of the same type will be required in each cycle of the oscillation. The frequency of the oscillation is given by:
\[ F_{\text{OSC}} = \frac{1}{2\Delta f} = \frac{I_D}{4C V_{THN}} \]  

(2)

3. RESULTS AND DISCUSSION

The circuit given by the figure 1 has been simulated using BSIM4 model with 50nm CMOS process. The parameters for simulation for this VCO are given in table 1. Figure 2 shows the plot between input voltage and frequency of the designed VCO. It shows that the input voltage and frequency of oscillation \(F_{\text{osc}}\) is linearly related. The centre frequency is 100MHz at the input voltage \(V_{\text{inCO}} = 0.45V\). The maximum frequency is 112MHz and minimum frequency is 86 MHz has been reported. The gain of the VCO is \(5.65 \times 10^9\) radians/ Vs. Figure 3 shows the simulated waveform of the source-coupled voltage controlled oscillator (VCO). Figure 4 shows simulated output waveform of the VCO after restoring the full logic levels. It shows that a 100MHz square wave is obtained at the input voltage of 0.45volt.

Table 1  
\textbf{Important Parameters of VCO for Simulation}

<table>
<thead>
<tr>
<th>Component of the VCO</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>N_5-N_6 (W/L)</td>
<td>30(\mu)m/1(\mu)m</td>
</tr>
<tr>
<td>N_7-N_8 (W/L)</td>
<td>10(\mu)m/10(\mu)m</td>
</tr>
<tr>
<td>N_3-N_4 (W/L)</td>
<td>100 (\mu)m/1 (\mu)m</td>
</tr>
<tr>
<td>P_1-P_2, N_2(W/L)</td>
<td>100 (\mu)m/1 (\mu)m</td>
</tr>
<tr>
<td>N_1(W/L)</td>
<td>200 (\mu)m/1 (\mu)m</td>
</tr>
<tr>
<td>R</td>
<td>55K</td>
</tr>
<tr>
<td>C</td>
<td>100F</td>
</tr>
</tbody>
</table>

CONCLUSIONS

In this paper the design of a highly linear source-coupled CMOS voltage controlled oscillator has been given. The centre frequency of the VCO is 100MHz at the input voltage of 0.45 volt with the maximum and minimum frequencies are 112 MHz and 86MHz respectively. The gain of the designed VCO is \(5.65 \times 10^9\) radians/Vs.

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