A LOW TO HIGH VOLTAGE TOLERANT LEVEL SHIFTER FOR POWER MINIMIZATION

Harpreet Kaur¹, & Arvind Rajput²

UIET, Panjab University, Chandigarh, E-mail: harpreet.banwait6@gmail.com

Abstract: A Level shifter used in multiple voltage digital circuits is presented. Level shifter allow for effective interfacing between voltage domains supplied by different voltage level. Usually conventional level shifter which can shift any voltage level signal to a desired higher level with low leakage current. In this level shifter we used multi VDD design techniques which give more design flexibility for low power system. In this paper we used high voltage tolerant level shifter for power minimization. Many application of this level shifter used in memory card, LCD, TV & mobile phones etc. This circuit is designed in 180nm technology and simulated on Tanner Tool Eda.

Keywords: Level shifter, conventional level shifter, high voltage tolerant circuit.

1. INTRODUCTION

To achieve high performance and high integration density, the transistor dimensions are aggressively scaled down in ultra deep submicron process while low power dissipation is achieved by scaling down the supply voltage.

With the wide applications of battery supplying devices, such as portable PC, cell phone and PDA, power consumption has become a critical design concern in today's VLSI circuit and system designs. In addition, approximately millions of transistors have been packed into a single chip in nanometer technologies. So the heat dissipation caused by huge power consumption becomes a problem that can adversely affect reliability and packaging cost of a design. These factors have attracted much attention on low power design of CMOS circuits and driven numerous research efforts to address various kinds of power reduction techniques[15]. Multiple supply voltages techniques have been proposed for low power design. With the use of two different supply voltages, it is possible that a low-voltage gate is made to drive a high-voltage one. This leads to the high output of the low-voltage gate cannot fully turn off the PMOS part of the high-voltage gate, so it forms a DC leakage path from the power source to ground. The DC leakage can lead to substantial power loss. To solve this problem, a level shifter is used at the interface of a low-voltage and high-voltage gates. The level shifter is a key circuit component in multi-voltage circuits and has important implementation[15]. For a chip-level DVS system, level shifters are required between core circuits and I/O circuits interface where low voltage logic signals from chip core are shifted to high voltage level at which pad ring is working. Since the level shifter circuit consumes power and has a considerable delay, how to optimize the performance to gain low power and small delay and how to minimize the number of level shifters are important in the voltage scaling technique. In this paper, we study different types of level shifter and also high voltage tolerant circuit.

1.1. Conventional Level Shifter

A conventional level shifter where inputs low supply voltage VddL and the output high supply voltage VddH are used. The two pmos transistors p₁₁ and p₁₂ act as a cross-coupled load.

Thick gate oxide transistor was used for n₁₁, n₁₂, p₁₁, and p₁₂ to overcome high voltage stress. Assuming that when the input signals (in) is at vss, n₁₁ turns Oᵣ and n₁₂ turns Oᵣ. Because of the positive feedback action of cross-coupled p₁₁ and p₁₂ node T₁ is pulled down to vss and node T₂ goes to VddH. No leakage current path exists between VddH and vss. Similarly, the operation reverses if input signal (in) switches to VddH, the following procedure is take place. N₁₁ turns Oᵣ and n₁₂ turns Oᵣ. N₁₁ pulls down
Finally the transition time from low voltage to high voltage is decided by the current driving capability of \( p_{11} \). Pull down nmos has to overcome the pmos latch action before the output change state, so the size of \( n_{11} \) and \( n_{12} \) are much larger than \( p_{11} \) and \( p_{12} \). [11]

The convention level shifter has two disadvantages in actual implementation. First, because of the thick gate oxide transistor’s \( (n_{11}, n_{12}) \) high threshold voltage, it can not operate at the core voltage \( V_{ddL} \) under 1V. Second, current driving capability of \( n_{11} \) and \( n_{12} \) are decided by core voltage \( V_{ddL} \), but those of \( p_{11} \) and \( p_{12} \) are controlled by the I/O voltage \( V_{ddH} \). So when I/O voltage \( V_{ddH} \) changes, it will make different current driving capability result in delay variation in level shifter. Therefore, it is not adequate for wide range voltage application in a given core voltage.

1.2. Single Supply Level Shifter

The needs for two voltage supply limit the physical placement of such level shifter to the boundary of high and low voltage designs which restricts the physical design flexibility. To address this, a novel level shifter which requires only one supply \( V_{ddH} \) to convert the low Voltage signal to the higher voltage has been proposed. It makes the placement much more flexible in the entire high voltage regions. Figure 2 shows the schematic diagram of single supply level shifter. The threshold drop (vt) across the nmos \( n_{1} \) provides a virtual \( V_{ddL} \) to the input inverter \( (p_{2}, n_{2}) \). The output stage is a half latch which pulls up the input of the inverter \( (p_{2}, n_{2}) \) to \( V_{ddH} \) in order to avoid leakage. When input signal \( (in) \) is HIGH, the voltage at node \( v \) is \( (V_{ddH} - vt) \) with the purpose of reducing gate to source voltage of \( p_{2} \) to turn it OFF. When the input signal \( (in) \) is LOW, the feedback transistor \( p_{4} \) turns \( Q_{N} \) so that charges node \( v \) to \( V_{ddH} \) to compensate the threshold drop. Hence the supply voltage of inverter \( (p_{2}, n_{2}) \) is dynamically switched between \( V_{ddH} - vt \) and \( V_{ddH} \) depending upon the input state.[11]

The biggest advantage of this level shifter is its flexible placement which enables efficient physical design of voltage islands. But, the single supply level shifter can suffer from higher leakage currents if input signal supply level is lower or lower or \( V_{ddH} \) is higher than input supply level by more than vt. So it is limited with wide range of input and output supplies. Also the diode connected transistor \( n_{1} \) limits the operating speed of the circuit.

1.3. High Voltage Tolerant Circuit using Conventional Level Shifter

A low to high voltage level shifter is required along with the some mechanism of preventing the MOSFET leakages. A high voltage tolerant level shifter is one of the configurations which solve these issues. The main approach used in this work is a high voltage tolerant level shifter[27]

On-chip voltage converters are becoming increasingly important for ultra-low voltage nanoscale memories. They include the reference voltage generator, the voltage down-converters, the voltage up-converter and negative voltage generator with charge pump circuits, and level shifters to adjust resultant voltage differences between internal blocks and between the internal core and I/O circuits. In the past, DRAMs and flash memories have required such voltage converters to ensure stable operations and retention characteristics of memory cells, and they will continue to need such converters. Even
future SRAM cells may need such converters for ensuring low sub threshold current and stable operation. For example, the raised voltage necessary for such memory cells must be kept high, independent of device scaling, to ensure data-retention characteristics, although the operating voltage for peripheral logic circuits can be scaled down with device scaling. Consequently, the voltage difference between memory cells and peripheral circuits will grow with device scaling.

In addition, interface circuits of chips must operate at quite a high external voltage, although some internal circuits using scaled devices can operate at another low external voltage. Moreover, in the near future, even some logic gates will have to operate at high voltages using raised (boosted) supply voltages and/or negative supply voltages, to manage sub threshold currents. These circumstances unavoidably call for stress voltage-immune circuits for the memory cell and its related circuits, interface-related circuits, and sub threshold-current sensitive circuits. In this paper we discuss the high-voltage tolerant circuit techniques for such circuits with using of conventional level shifter and single supply levels shifter[8].

Figure 3: High Voltage Tolerant Circuit

Device scaling causes the reliability problem, such as device-parameter degradation due to hot carrier, breakdown of gate oxide due to high electric field, and punch through. Thus, releasing the stress-voltage is indispensable for MOSTs in circuits operating at high stress voltages. The following circuit techniques are proposed for the above problems. This circuit has a protection device only for an NMOST because of the above reasons. Here, MN2 is the protection device. The series connection of two NMOSTs halves the drain-source voltage of each NMOST and reduces hot-carrier injection.

Figure 4: High Tolerant with Single Supply Level Shifter

A level shifter circuit using the high-voltage tolerant technique this circuit converts the input signal with a voltage swing of $V_{DD1}$ into the output signal with a larger swing of $V_{DD2}$. This circuit consists of two sets of the inverters shown in Fig. 3. The PMOSTs $M_{P1}$ and $M_{P3}$ are cross-coupled, while NMOSTs $M_{N1}$ and $M_{N3}$ receive complementary input signals. The differences include that thick gate-oxide MOSTs are used except for the input NMOSTs $M_{N1}$, $M_{N3}$, and that the gates of $M_{P2}$, $M_{P4}$, $M_{N2}$ and $M_{N4}$ are supplied with the input signal instead of dc voltage.

2. SIMULATION RESULTS

A logic swinging between 1.8V and 0 is applied at input signal (in) and the level shifted signals swinging between 3.6V and 0 are obtained at output signal (out). At the end of the paper comparing all level shifter.

3. SIMULATION RESULTS

<table>
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<th></th>
<th>PRM</th>
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<th>CMLS</th>
<th>HTCLS</th>
<th>HTSLS</th>
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<td>7mW</td>
<td>2.0mW</td>
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<tr>
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4. CONCLUSION AND FUTURE WORK

In this paper, several level shifters have been evaluated to traditional CMOS levels. One single supply circuit with high voltage tolerant circuit was included in the evaluation as well as three level shifters discussed in this paper. All these circuits were evaluated in terms of power and speed performance. Simulation results show proper shifting of a lower supply logic signal to higher supply logic without consuming any steady state current. Low power techniques such as VTCMOS and MTCMOS can be used to minimize power dissipation the future scope of this project. So, we can use some other techniques to reduce leakage, for example-multiple threshold CMOS technique, variable threshold CMOS technique. New circuit families which are more efficient and power saving can also be used to reduce the power. The configuration used in this thesis can be implemented and analyzed at nanometer technology nodes such as 130nm, 90nm

REFERENCES


[28] www.mosis.org